



## Research paper

## GPU performance analysis of a nodal discontinuous Galerkin method for acoustic and elastic models

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## ABSTRACT

Finite element schemes based on discontinuous Galerkin methods possess features amenable to massively parallel computing accelerated with general purpose graphics processing units (GPUs). However, the computational performance of such schemes strongly depends on their implementation. In the past, several implementation strategies have been proposed. They are based exclusively on specialized compute kernels tuned for each operation, or they can leverage BLAS libraries that provide optimized routines for basic linear algebra operations. In this paper, we present and analyze up-to-date performance results for different implementations, tested in a unified framework on a single NVIDIA GTX980 GPU. We show that specialized kernels written with a one-node-per-thread strategy are competitive for polynomial bases up to the fifth and seventh degrees for acoustic and elastic models, respectively. For higher degrees, a strategy that makes use of the NVIDIA cuBLAS library provides better results, able to reach a net arithmetic throughput 35.7% of the theoretical peak value.

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## 1. Introduction

High-performance compute resources are used intensively in modern computational seismology for applications including earthquake simulation and seismic imaging. State-of-the-art compute clusters consist of massively parallel many-core central processing units (CPUs) with graphics processing units (GPUs) or coprocessors to provide a performance boost. Computing on GPUs has been made accessible to the scientific community thanks to programming frameworks that expand languages already widely used (e.g. C, C++ or Fortran). However, to fully leverage the capabilities of GPUs, applications must be developed taking into account specifics of each architecture. It is therefore critical to develop computational algorithms that can be efficiently implemented on these architectures.

In computational seismology, several implementations have been proposed for numerical methods suitable for GPUs coprocessors. Examples include tuned implementations for finite-difference schemes (Michea and Komatitsch, 2010; Weiss and Shragge, 2013; Abdelkhalek et al., 2012; Rubio et al., 2014) or finite-element schemes (Heinecke et al., 2014; Komatitsch et al., 2009, 2010; Mu et al., 2013; Modave et al., 2015). Nowadays, the finite-difference schemes are the most widely used, and a large

literature is available (see e.g. Virieux et al., 2011 for a review). However, the stencil based reconstruction used in finite difference methods is not ideally suited to resolving wave propagation in realistic physical heterogeneous media typically suffering from loss of accuracy (Symes and Vdovina, 2009). By contrast, finite-element methods based on unstructured meshes are better suited to handle such material interfaces. Several variants have been investigated, such as spectral finite-element methods (Komatitsch and Vilotte, 1998; Komatitsch and Tromp, 1999), continuous mass-lumped finite-element methods (ChinJoeKong et al., 1999; Cohen et al., 2001) or discontinuous Galerkin (DG) methods (Dumbser and Käser, 2006; de la Puente et al., 2007; Collis et al., 2010; Etienne et al., 2010; Krebs et al., 2014; Mercier and Glinsky, 2015). In contrast to the standard schemes, the mentioned methods do not require the solution of large sparse linear systems of equations, and it is possible to use explicit time-stepping schemes. The DG approach, in particular, provides a framework that is both flexible for multi-scale modeling and appears to be well suited for GPU accelerated computing. First, it can easily handle local time-stepping strategies (Warburton, 2008; Dumbser and Käser, 2009; Baldassari et al., 2011; Minisini et al., 2013), and hybrid discretizations can be deployed by mixing different discretization orders and several kinds of elements (Kirby et al., 2000; Dumbser and Käser, 2009; Etienne et al., 2010; Chan et al., 2015). Then, the weak element-to-element coupling and the dense algebraic operations required per element are suitable for parallel multi-threading computations with GPUs (Klöckner et al., 2009).

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Discontinuous Galerkin schemes can be implemented in different ways for GPU computing. Klöckner et al. (2009) proposed an implementation for first-order wave systems discretized using a nodal DG scheme. This implementation has been successfully adapted to several physical contexts (Gödel et al., 2010; Gandham et al., 2015; Modave et al., 2015), and we have recently presented an application for reverse-time migration with multi-rate time-stepping and GPU clusters (Modave et al., 2015a). Alternatively, Fuhry et al. (2014) have proposed an implementation for two-dimensional problems with a modal DG scheme. All these implementations partition the computational work into tailored GPU kernels, which are optimized separately in order to improve performance. A key difference between the approaches of Klöckner et al. (2009) and Fuhry et al. (2014) is the programming strategy of kernels: each thread performs computations corresponding to one node and to one element, respectively. On the other hand, Witherden et al. (2014, 2015) recently developed an implementation based on a nodal DG method for applications of fluid dynamics. This implementation, named PyFR, makes use of external BLAS libraries that provide linear algebra routines optimized for hardware devices. Such a strategy has been successfully used for CPU computing (Chevaugne et al., 2005; Hesthaven and Warburton, 2002; Marchandise et al., 2006; Vos et al., 2010).

In this paper, we investigate and evaluate three strategies to implement time-domain DG schemes for GPU computing. All these strategies have been compared for three-dimensional acoustic and elastic cases with a unique computational framework. They were programmed in C++ using CUDA 7.5 through the abstract framework OCCA (Medina, 2014), and tested on a single Nvidia GTX980. We have tested one-element-per-thread and one-node-per-thread strategies, as well as a strategy that makes use of an external BLAS library. In this work, we have used the generalized single precision matrix-multiplication (SGEMM) routine of NVIDIA's cuBLAS library (NVIDIA Corporation, 2015a). We show that, similarly to CPU implementations (Vos et al., 2010), the best GPU implementation depends on the polynomial degree. The one-node-per-thread tailored kernels provided the best runtime for small degree, while the implementation with SGEMM is better for higher degrees.

This paper is organized as follows. In Section 2, we present the mathematical models for acoustic and elastic wave propagation, and we describe the nodal discontinuous Galerkin method and the time-stepping scheme. In Section 3, key aspects of GPU hardware and GPU programming are summarized, and all the implementations are described. Section 4 is dedicated to performance results and comparisons. We discuss the optimization of the SGEMM routine for the DG operations, and we analyze its performance using the roofline model. The implementations are then compared, and all the kernels are systematically profiled.

## 2. Discontinuous Galerkin schemes

We consider acoustic and isotropic elastic wave models discretized with a nodal discontinuous Galerkin method in space and on a third-order Adam–Bashforth method in time. We assume the physical coefficients to be constant over each mesh cell and discontinuous at interfaces. The variational forms of the models and the schemes are presented in Sections 2.1 and 2.2, respectively.

### 2.1. Physical models and variational forms

Acoustic waves are governed by the pressure-velocity system, which reads

$$\begin{aligned}\frac{\partial p}{\partial t} + \rho c^2 \nabla \cdot \mathbf{v} &= 0, \\ \rho \frac{\partial \mathbf{v}}{\partial t} + \nabla p &= 0,\end{aligned}$$

with the pressure  $p(\mathbf{x}, t)$ , the velocity  $\mathbf{v}(\mathbf{x}, t)$ , the density  $\rho(\mathbf{x})$  and the phase velocity  $c(\mathbf{x})$ . For each mesh cell  $D_k$ , we consider the variational form

$$\begin{aligned}\int_{D_k} \frac{\partial p}{\partial t} \psi \, d\mathbf{x} &= - \int_{D_k} \rho c^2 \nabla \cdot \mathbf{v} \psi \, d\mathbf{x} - \int_{\partial D_k} p_p \psi \, d\mathbf{x} \\ \int_{D_k} \frac{\partial \mathbf{v}}{\partial t} \psi \, d\mathbf{x} &= - \int_{D_k} \frac{1}{\rho} \nabla p \cdot \psi \, d\mathbf{x} - \int_{\partial D_k} p_v \mathbf{n} \cdot \psi \, d\mathbf{x}\end{aligned}$$

where  $\psi(\mathbf{x})$  is a test function,  $p_p(\mathbf{x})$  and  $p_v(\mathbf{x})$  are penalty terms. The penalty terms corresponding to upwind fluxes provided by a one-dimensional Riemann solver are given by (see e.g. Hesthaven and Warburton, 2007; Modave et al., 2015a)

$$p_p = -(\rho c^2)^- k_c \alpha_c,$$

$$p_v = c^- k_c \alpha_c,$$

with  $\alpha_c = [[p]] - (\rho c)^+ [[v_n]]$ ,  $k_c = 1/\{\rho c\}$  and the semi-jumps defined as  $[[p]] = (p^+ - p^-)/2$  and  $[[v_n]] = (\mathbf{v}^+ - \mathbf{v}^-) \cdot \mathbf{n}/2$ . The brackets  $\{\cdot\}$  denotes the mean value at the interface.

For isotropic media, elastic waves can be simulated with the velocity-stress system, which reads

$$\begin{aligned}\frac{\partial \boldsymbol{\sigma}}{\partial t} &= \lambda (\nabla \cdot \mathbf{v}) \mathbf{I} + 2\mu \text{sym}(\nabla \mathbf{v}), \\ \rho \frac{\partial \mathbf{v}}{\partial t} &= \nabla \cdot \boldsymbol{\sigma},\end{aligned}$$

with the stress tensor  $\boldsymbol{\sigma}(\mathbf{x}, t)$  and the Lamé parameters  $\lambda(\mathbf{x})$  and  $\mu(\mathbf{x})$ . This system supports pressure waves and shear waves, which the phase velocities are

$$c_p = \sqrt{(\lambda + 2\mu)/\rho},$$

$$c_s = \sqrt{\mu/\rho},$$

respectively. We consider the variational form

$$\begin{aligned}\int_{D_k} \frac{\partial \boldsymbol{\sigma}}{\partial t} \psi \, d\mathbf{x} &= \int_{D_k} \lambda (\nabla \cdot \mathbf{v}) \mathbf{I} + 2\mu \text{sym}(\nabla \mathbf{v}) \psi \, d\mathbf{x} + \int_{\partial D_k} \mathbf{P}_\sigma \psi \, d\mathbf{x}, \\ \int_{D_k} \frac{\partial \mathbf{v}}{\partial t} \psi \, d\mathbf{x} &= \int_{D_k} \frac{1}{\rho} (\nabla \cdot \boldsymbol{\sigma}) \psi \, d\mathbf{x} + \int_{\partial D_k} \mathbf{P}_v \psi \, d\mathbf{x}\end{aligned}$$

where the upwind fluxes provided by an exact Riemann solver are given by Wilcox et al. (2010)

$$\mathbf{P}_\sigma = k_p \alpha_p \lambda^- \mathbf{I} + 2(k_p \alpha_p - k_s \alpha_s) \mu^- \mathbf{N} + 2k_s \mu^- \text{sym}(\mathbf{n} \otimes \alpha_s),$$

$$\mathbf{P}_v = (k_p \alpha_p c_p^- - k_s \alpha_s c_s^-) \mathbf{n} + k_s c_s^- \alpha_s,$$

with

$$\alpha_p = [\sigma_{nn}] + (\rho c_p)^+ [[v_n]], \quad k_p = 1/\{\rho c_p\}, \quad [\sigma_{nn}] = \mathbf{n} \cdot (\boldsymbol{\sigma}^+ - \boldsymbol{\sigma}^-) \cdot \mathbf{n}/2,$$

$$\alpha_s = [\sigma_{nn}] + (\rho c_s)^+ [[v_n]], \quad k_s = 1/\{\rho c_s\}, \quad [\sigma_{nn}] = (\boldsymbol{\sigma}^+ - \boldsymbol{\sigma}^-) \cdot \mathbf{n}/2,$$

$$\alpha_s = [\boldsymbol{\sigma} \mathbf{n}] + (\rho c_s)^+ [[\mathbf{v}]], \quad \mathbf{N} = \mathbf{n} \otimes \mathbf{n}, \quad [[\mathbf{v}]] = (\mathbf{v}^+ - \mathbf{v}^-)/2.$$

### 2.2. Numerical schemes

The approximate fields are built on a spatial mesh of the computational domain  $\Omega \subset \mathbb{R}^3$ , made of  $K$  non-overlapping tetrahedral cells,  $\Omega = \bigcup_k D_k$ , where  $D_k$  is the  $k$ th cell. For the nodal discontinuous Galerkin method, all the scalar fields and the Cartesian components of vector and tensor fields are approximated by piecewise polynomial functions. The discrete unknowns correspond to the values of fields at nodes distributed over the surface and interior of an element (Hesthaven and Warburton, 2002,

2007). Over each cell  $D_k$ , the approximate fields can then be represented by

$$\mathbf{q}_k(\mathbf{x}, t) = \sum_{n=1}^{N_p} \mathbf{q}_{k,n}(t) \ell_{k,n}(\mathbf{x}), \quad \forall \mathbf{x} \in D_k, \quad (1)$$

where  $N_p$  is the number of nodes per element,  $\mathbf{q}_{k,n}(t)$  is the values of fields at node  $n$  of element  $k$ , and  $\ell_{k,n}(\mathbf{x})$  is the associated multivariate Lagrange polynomial function. In this work, the position of nodes are chosen using the warp-and-blend technique (Warburton, 2006). The number of nodes for each element is given by  $N_p = (N+1)(N+2)(N+3)/6$ , where  $N$  is the maximal order of polynomial functions.

The semi-discrete equations are obtained by substituting the approximate representation of fields into the weak form, and using the Lagrange polynomials as test functions. For each element  $k$ , a system of equations can then be expressed as

$$\frac{d\mathbf{q}_k}{dt} = \mathbf{r}_k, \quad (2)$$

where the right-hand side vector is defined as

$$\mathbf{r}_k = \sum_{i=1}^3 \sum_{j=1}^3 g_{k,i,j}^{\text{vol}} \mathbf{D}_j \mathbf{f}_{j,k} + \sum_{f=1}^{N_{\text{faces}}} g_{k,f}^{\text{sur}} \mathbf{L}_f \mathbf{p}_{k,f}, \quad (3)$$

where  $N_{\text{faces}}$  is the number of faces,  $\mathbf{f}_{j,k}$  correspond to the physical flux in the  $x_j$ -direction for all the nodes of element  $k$ , and the vector  $\mathbf{p}_{k,f}$  contains the penalty terms for all the nodes belonging to face  $f$ . The first term of the right-hand side vector in Eq. (3) corresponds to the volume integrals of the variational form, while the second term corresponds to the surface integrals. The matrices  $\mathbf{D}_j$  and  $\mathbf{L}_f$  are, respectively, the differentiation matrices and the lifting matrices of the reference element. The geometric factors  $g_{k,i,j}^{\text{vol}}$  and  $g_{k,f}^{\text{sur}}$  depend on the shape of each element. The definitions of these matrices and factors, and a complete derivation of the semi-discrete equations are given in Modave et al. (2015a).

The global semi-discrete scheme is simply built by combining the local systems of all elements. We use the classical third-order Adams–Bashforth formula for time discretization. At each iteration, the discrete unknowns of all the elements are updated according to

$$\mathbf{q}_k^{m+1} = \mathbf{q}_k^m + \Delta t \sum_{s=1}^3 a_s \mathbf{r}_k^{m-s+1}, \quad (4)$$

with  $a_1 = 23/12$ ,  $a_2 = -16/12$  and  $a_3 = 5/12$ , and where  $m$  is the time index. This formula only depends on the right-hand side vector  $\mathbf{r}_k$  at the three time levels  $t^m$ ,  $t^{m-1}$ ,  $t^{m-2}$ . For each step, this vector is thus computed with the values of unknowns local to the element, as well as those of the neighboring element at each interface.

### 3. Implementations for GPU computing

We consider three different GPU-based implementations of DG schemes. Each has been programmed in a C++ code using CUDA 7.5 through the abstract framework OCCA (Medina, 2014), and tested with a single NVIDIA GTX980. In Section 3.1, we summarize key characteristics of NVIDIA's GPU architecture and CUDA programming. Specifications corresponding to the NVIDIA GTX980 are mentioned in brackets [...]. We present two implementations based exclusively on specialized kernels in Section 3.2. In Section 3.3, we propose an alternative strategy that makes use of the basic linear algebra subroutine SGEMM, from NVIDIA's cuBLAS library, optimized for dense algebraic operations on GPU.

#### 3.1. GPU architecture and GPU programming

Heterogeneous computing systems consist of central processing units (CPUs) complemented with sidcar graphics processing units (GPUs), each with its own memory space. The programming framework CUDA (NVIDIA Corporation, 2015b; Cheng et al., 2014) provides extensions to the C programming language to allocate/deallocate storage in the global memory of GPU, to manage memory transfers between the CPU memory and the GPU memory, and to invoke *kernels*—the codes that run on the GPU. In our implementations, memory allocations and CPU–GPU data transfers are performed only at the beginning of the computation, and during the time stepping only when the solution must be exported for checkpointing or halo exchanges. The main challenge consists in optimizing the execution of tasks to be performed by the GPU.

The execution is based on the *single instruction multiple threads* (SIMT) model, where many *threads* are executed concurrently by the GPU. In the programming framework CUDA, threads are grouped into *thread blocks* [max. 1024 threads per thread block], which compose the *grid*. At the hardware level, each *thread block* is assigned to one *streaming multiprocessor* (SM) as the kernel executes [16 SMs on chip with 128 cores per SM], and successive threads of each thread block are grouped into *warps* [32 threads per warp]. Ideally, all the threads of a warp must perform the same instructions to avoid *warp divergence*. Warp schedulers manage the execution of warps, eventually context switching between warps to avoid the SM from stalling [max. 64 active warps per SM] due to high device memory load and store latencies. The percentage of active warps to the maximum theoretical number of active warps is called *occupancy*. It is generally advised that the number of threads per thread block should be chosen to be a multiple of 32 to maximize the occupancy (NVIDIA Corporation, 2015c), though, strategies with low occupancy can also be efficient (Volkov, 2010).

The GPU has a deep non-uniform memory architecture with a hierarchy of memory spaces, each with different purposes and characteristics that indicate their best use cases. *Global memory* [4 GB] is the largest on device memory space and is accessible by all the threads, in all warps, in all thread-blocks, in all kernels. The bandwidth of this memory [max. 224 GB/s] is generally a bottleneck. Common strategies to maximize usage of global memory include hiding latency due to data transfer by overlapping memory load and store requests with computations, and making coalesced memory transfers by requesting contiguous blocks of data that are page aligned to maximize the utilization of the memory bus. Similarly to CPUs, GPUs have also a system of lower-latency *caches* (L2 cache [2 MB] and L1 cache [48 KB per SM]), which allow reuse of data previously fetched from the global memory. These caches cannot be programmed at the level of CUDA, and their use is determined by the streaming multiprocessor cache management system.

*Shared memory* (smem) [96 KB per SM, max. 48 KB per thread block] is a relatively low latency memory that can be accessed by threads of a thread block, providing a scratch pad for thread-block level data sharing and collaboration. Shared memory can be considered as a programmable cache, where memory storage is allocated at the thread block execution, and released when it is finished. Shared memory accesses are served by 32 independent memory managers. Shared memory is organized into banks that are interleaved in the logical indexing of the memory addresses. Efficient data transactions are served by the shared memory managers if all threads in a warp that access shared memory do so by accessing the 32 banks. Finally, data that are local to each thread are stored in 32-bit *registers* [64 K per SM, max. 255 per thread] that provide very low latency accesses. When the number of registers is insufficient to contain all the register variables for all the threads in a thread-block the *spilled register* data are stored in

the local memory space, that is mapped to global memory and cached in L1 and L2 increasing the latency. The storage allocated for spilling registers is called *local memory* (lmem). NVIDIA's GPUs also have constant memory and texture memory, but they are not used in this work.

### 3.2. Implementations with specialized kernels

The operations to perform in the DG implementations can be partitioned into several kernels, which provides flexibility to optimize each task considering its own characteristics. For each time-step update, the right-hand side vector (3) must be computed at the current time, and the values of fields must be updated with the update scheme (4). Following previous works (Gödel et al., 2010; Fuhry et al., 2014; Gandham et al., 2015; Modave et al., 2015a), we consider implementations with three main kernels: the *volume kernel* and the *surface kernel* compute, respectively, the volume terms and the surface terms of the right-hand side vector, while the *update kernel* performs the time stepping. A similar partition of operations into tailored kernels has also been successfully tested for computing with coprocessors (Heinecke et al., 2014). We have tested implementations based on two different strategies: in all the kernels, each thread deals with the computations corresponding to one element (*one-element-per-thread* strategy) or one node (*one-node-per-thread* strategy). These implementations are based on the work of Fuhry et al. (2014) and Klöckner et al. (2009). In the following we describe key aspects of memory storage and kernel programming with these strategies.

For both considered implementations, all the required data are stored in global memory: the array  $Q$  with the values of fields at all the nodes, the array  $Q_f$  with the values of traces ( $p$  and  $\mathbf{n} \cdot \mathbf{u}$  for the acoustic case, and  $\mathbf{u}$  and  $\sigma \mathbf{n}$  for the elastic case) at all the face nodes, the arrays  $R_0$ ,  $R_{-1}$  and  $R_{-2}$  with the values of the right-hand-side vector corresponding to the current and two previous time steps, the arrays  $D_i$  and  $L$  with the differentiation and lift matrices, and specific arrays for the geometric factors and physical coefficients. The granularity of storage depends on the implementation strategy. With the one-element-per-thread strategy, successive threads have to fetch/store values corresponding to successive elements. It then is advantageous to store all the arrays with the element index  $k$  as the finest level of granularity, which enables coalescing data transfers with global memory (Fuhry et al., 2014). By contrast, with the one-node-per-thread strategy, successive threads deal with successive nodes. A granularity with the node index  $n$  at the finest level then is the best choice (Modave et al., 2015a). Dimensions and granularity of the main arrays are given in Table 1.

We describe the tasks that must be performed by each kernel. For the acoustic case, the right-hand side vector (3) can be rewritten as

$$\mathbf{r}_k^p = -\rho_k c_k^2 \sum_{j=1}^3 \mathbf{D}_j \left[ \sum_{i=1}^3 g_{k,i,j}^{\text{vol}} \mathbf{q}_k^{v_i} \right] - \mathbf{L} \mathbf{p}_k^p, \quad (5)$$

$$\mathbf{r}_k^{v_i} = -\frac{1}{\rho_k} \sum_{j=1}^3 g_{k,i,j}^{\text{vol}} [\mathbf{D}_j \mathbf{q}_k^p] - \mathbf{L} \mathbf{p}_k^{v_i}, \quad \text{for } i = 1, 2, 3, \quad (6)$$

where the lift matrices have been merged into  $\mathbf{L}$ , and the penalty vectors  $\mathbf{p}_k^{[p,v_i]}$  contain the penalty terms multiplied with the geometric factors for all the face nodes of the element. The superscripts  $p$  and  $v_i$  denote vectors with values corresponding to the pressure  $p$  and the Cartesian component of velocity  $v_i$ . Using similar notations, the right-hand side vector of the elastic case can be rewritten as

**Table 1**

List of main arrays stored in the global memory of the device. Dimensions are given from the coarsest to the finest granularity of storage.  $N_p$ ,  $N_{fp}$ ,  $N_{\text{faces}}$  and  $K$  are, respectively, the number of nodes per element, the number of nodes per face, the number of faces per element, and the number of elements in the mesh.  $N_{\text{fields}}$  and  $N_{\text{traces}}$  are the number of fields and traces, respectively.

Name	Symbol	Granularity one-element-per-thread	Granularity one-node-per-thread
Values of fields at nodes	$Q$	$N_{\text{fields}} \cdot N_p \cdot K$	$K \cdot N_{\text{fields}} \cdot N_p$
Values of traces at face nodes	$Q_f$	$N_{\text{traces}} \cdot N_{\text{faces}} \cdot N_{fp} \cdot K$	$K \cdot N_{\text{traces}} \cdot N_{\text{faces}} \cdot N_{fp}$
Right-hand side terms	$R_{\{0,-1,-2\}}$	$N_{\text{fields}} \cdot N_p \cdot K$	$K \cdot N_{\text{fields}} \cdot N_p$
Differentiation matrices	$D_i$	$N_p^2$	$N_p^2$
Merged lift matrix	$L$	$N_{\text{faces}} \cdot N_{fp} \cdot N_p$	$N_{\text{faces}} \cdot N_{fp} \cdot N_p$

$$\begin{aligned} \mathbf{r}_k^{v_i} &= \frac{1}{\rho_k} \sum_{n=1}^3 \mathbf{D}_n \left[ \sum_{m=1}^3 g_{k,m,n}^{\text{vol}} \mathbf{q}_k^{\sigma_{im}} \right] + \mathbf{L} \mathbf{p}_k^{v_i}, \quad \text{for } i = 1, 2, 3, \\ \mathbf{r}_k^{\sigma_{ij}} &= \delta_{ij} \lambda_k \sum_{m=1}^3 \sum_{n=1}^3 g_{k,m,n}^{\text{vol}} [\mathbf{D}_n \mathbf{q}_k^{v_m}] \\ &\quad + \mu_k \sum_{m=1}^3 \left( g_{k,i,m}^{\text{vol}} [\mathbf{D}_m \mathbf{q}_k^{v_j}] + g_{k,m,i}^{\text{vol}} [\mathbf{D}_i \mathbf{q}_k^{v_m}] \right) + \mathbf{L} \mathbf{p}_k^{\sigma_{ij}}, \\ &\quad \text{for } i, j = 1, 2, 3. \end{aligned}$$

The volume kernel performs element-wise tasks corresponding to the volume terms, which are the first terms of Eqs. (5) and (6) in the acoustic case. For each element, the values of fields are fetched from the array  $Q$ , and the main algebraic operations are linear combinations and six matrix–vector products with squared matrices of size  $N_p \times N_p$ . The surface kernel computes the penalty terms and performs the matrix–vector products for the second terms of Eqs. (5) and (6). In both volume and surface kernels, direct matrix–vector products are implemented. Let us mention that alternative DG methods with sparse elemental matrices can leverage sparse matrix–vector products (see e.g. Breuer et al., 2014; Chan and Warburton, 2015). The implementation of the surface kernel is trickier because computing the penalty terms requires the values of traces at face nodes corresponding to both sides of the interface (i.e. values for the current element and its neighbors), which leads to erratic memory accesses when fetching neighbor values. We use a mapping array that, for each face node, gives the location of the first trace corresponding to the neighbor element in the array  $Q_f$ . For each element, the surface kernel then loads both local and neighbor values of traces from the array  $Q_f$ , computes the penalty terms and multiplies them with geometric factors. The obtained values are then used in the merged matrix–vector product with a rectangular matrix of size  $N_p \times N_{\text{faces}} N_{fp}$  and a vector of size  $N_{\text{faces}} N_{fp}$ . Both volume and surface kernels accumulate the final right-hand side terms in the current right-hand side array  $R_0$ . The update kernel loads all the right-hand side arrays, updates the fields values in the array  $Q$  by performing the time-stepping, and updates the trace values in the array  $Q_f$ .

For the one-element-per-thread strategy, all kernels run with 256 threads per thread block. That number of threads has been suggested by Fuhry et al. (2014), and is also optimal for our implementation. For both volume and surface kernels, the elemental matrices (differentiation and lift) are stored in global memory and prefetched into shared memory by all the threads in collaborative way (successive threads fetch successive values). Let us mention that, in the implementation of Fuhry et al. (2014), the elemental matrices are stored in constant memory, and each value is fetched during the matrix–vector products. This strategy was however less



**Table 2**

Memory transfers performed by the volume and surface kernels. Fetched data are transferred when required, while prefetched data are loaded at the beginning of each kernel execution. The temporary array stores the vectors to be used in the matrix–vector products, which are the penalty vectors for the surface kernel.

Name	Memory transfer one-element-per- thread	Memory transfer one-node-per-thread
Fields and traces	Fetch into registers	Fetch into registers
Temporary array	Store in registers	Store in shared memory
Geometric and physical factors	Prefetch into registers	Prefetch into shared memory
Elemental matrices	Prefetch into shared memory	Fetch into registers

efficient in our case. The geometric factors, physical parameters and fields/traces, which are local to each element, are stored in registers. The final values of the right-hand side terms are stored in temporary arrays before being transferred to local memory using coalesced data transfers. While this implementation uses a lot of registers, leading to spilling registers for high polynomial degree, it provides the best runtime with this strategy. The kinds of memory transfer are summarized in Table 2.

With the one-node-per-thread strategy, threads collaborate to perform the computations required for each element. For all the kernels, each thread block deals with several elements, which allow us to have a reasonable number of threads per thread block for small polynomial degree. Therefore, we have  $K_{\text{blkV}}N_p$  threads per thread block for the volume kernel,  $K_{\text{blkS}} \max(N_p, N_{\text{faces}}N_{\text{fp}})$  for the surface kernel, and  $K_{\text{blkU}}N_p$  for the update kernel. The numbers of elements per thread block,  $K_{\text{blkV}}$ ,  $K_{\text{blkS}}$  and  $K_{\text{blkU}}$ , must be tuned. This implementation make use of shared memory to store temporary arrays with values that are useful for different threads. For more details about this implementation, we refer to our previous paper (Modave et al., 2015a).

### 3.3. Implementations with SGEMM routine

We investigate an alternative implementation which makes use of an extern BLAS library. Such library provides linear algebra routines that are tuned for specific hardware devices. In our computational procedure, the matrix–vector products of Eqs. (5) and (6) can be merged into global matrix–matrix products, which are BLAS-3 operations. They will be performed here with the SGEMM routine of the cuBLAS library developed by Nvidia (2015a). We describe hereafter the procedure only for the acoustic case, which can be straightforwardly adapted to the elastic case.

In order to integrate global matrix–matrix products in the computational procedure, we derive an alternative partition of tasks. The computation of the right-hand side terms can be rewritten with global operations. By merging Eqs. (5) and (6) for all the elements, we have

$$\mathbf{R}^p = \sum_i \mathbf{D}_i \mathcal{L}_i^p(\mathbf{Q}^v) + \mathbf{L}^p, \quad (7)$$

$$\mathbf{R}^v = \mathcal{L}^v(\mathbf{D}_1 \mathbf{Q}^p, \mathbf{D}_2 \mathbf{Q}^p, \mathbf{D}_3 \mathbf{Q}^p) + \mathbf{L}^v, \quad (8)$$

where  $\mathbf{Q}^{[p,v]}$ ,  $\mathbf{P}^{[p,v]}$  and  $\mathbf{R}^{[p,v]}$  are matrices for which the  $k$ th column corresponds, respectively, to the values of fields, the penalty terms and the right-hand side vectors of element  $k$ . The operators  $\mathcal{L}_i^p$  and  $\mathcal{L}^v$  abstract the linear combinations to perform for the volume terms. A rapid study of Eqs. (7) and (8) leads to the new partition of tasks:

1. computation of the *gradient* matrix–matrix product for Eq. (8)

[SGEMM routine]:

$$\begin{bmatrix} \mathbf{D}_1 \\ \mathbf{D}_2 \\ \mathbf{D}_3 \end{bmatrix} \mathbf{Q}^p \rightarrow \begin{bmatrix} \mathbf{Q}_1^{\text{tmp}} \\ \mathbf{Q}_2^{\text{tmp}} \\ \mathbf{Q}_3^{\text{tmp}} \end{bmatrix}, \quad (\text{or } \mathbf{D}_{\text{grad}} \mathbf{Q}^p \rightarrow \mathbf{Q}^{\text{tmp}}) \quad (9)$$

2. computation of the linear combinations for the volume terms [volume kernel]:

$$\mathcal{L}^v(\mathbf{Q}_1^{\text{tmp}}, \mathbf{Q}_2^{\text{tmp}}, \mathbf{Q}_3^{\text{tmp}}) \rightarrow \mathbf{R}^v, \\ \mathcal{L}_i^p(\mathbf{Q}^v) \rightarrow \mathbf{Q}_i^{\text{tmp}}, \quad \text{for } i = 1, 2, 3,$$

3. computation of the *divergence* matrix–matrix product for Eq. (7) [SGEMM routine]:

$$\begin{bmatrix} \mathbf{D}_1 & \mathbf{D}_2 & \mathbf{D}_3 \end{bmatrix} \begin{bmatrix} \mathbf{Q}_1^{\text{tmp}} \\ \mathbf{Q}_2^{\text{tmp}} \\ \mathbf{Q}_3^{\text{tmp}} \end{bmatrix} \rightarrow \mathbf{R}^p, \quad (\text{or } \mathbf{D}_{\text{div}} \mathbf{Q}^{\text{tmp}} \rightarrow \mathbf{R}^p) \quad (10)$$

4. computation of penalty vectors and storage in arrays  $\mathbf{P}^p$  and  $\mathbf{P}^v$  [surface kernel],
  5. computation of the *lift* matrix–matrix products and addition to the right-hand side arrays [ $2 \times$  SGEMM routine]:
- $$\mathbf{L}^p + \mathbf{R}^p \rightarrow \mathbf{R}^p, \\ \mathbf{L}^v + \mathbf{R}^v \rightarrow \mathbf{R}^v,$$
6. update of fields and traces with the time stepping scheme [update kernel].

In this new procedure, the first three operations compute the volume terms, the next two compute the surface terms, and the latter performs the update. The procedure requires three kernels and four calls of the SGEMM routine. We describe hereafter the arrays that must stored in global memory, the different settings for the SGEMM routine, and the kernels.

In comparison with the previous implementations, arrays  $\mathbf{Q}_i^{\text{tmp}}$  and  $\mathbf{P}^{[p,v]}$  have been introduced to store intermediate results, which was not necessary before since these intermediate results were immediately used to compute matrix–vector products. For the sake of clarity, the fields, traces and right-hand side terms are stored in two set of arrays, one for the pressure ( $\mathbf{Q}^p$ ,  $\mathbf{Q}^f$  and  $\mathbf{R}^p$ ) and the other for the velocity ( $\mathbf{Q}^v$ ,  $\mathbf{Q}^f$  and  $\mathbf{R}^v$ ). To efficiently use the SGEMM routine, the arrays  $\mathbf{Q}_i^{\text{tmp}}$  are merged into the array  $\mathbf{Q}^{\text{tmp}}$ , and the differentiations arrays  $\mathbf{D}_i$  are stored into two merged arrays, the gradient array  $\mathbf{D}_{\text{grad}}$  and the divergence array  $\mathbf{D}_{\text{div}}$ . The granularity of storage follows the one-node-per-thread strategy of the previous section, with the node index  $n$  at the finest level. This is required to use the SGEMM routine.

Conforming to BLAS terminology, the SGEMM routine computes the general matrix multiplication  $\mathbf{C} = \alpha \mathbf{A} \mathbf{B} + \beta \mathbf{C}$ , where  $\mathbf{A}$ ,  $\mathbf{B}$  and  $\mathbf{C}$  are, respectively,  $m \times k$ ,  $k \times n$  and  $m \times n$  matrices and  $\alpha$  and  $\beta$  are scalars. The memory storage of arrays must be column-major for the matrix  $\mathbf{C}$ , and either column-major or row-major for the others. They can be padded in order to improve computational performances. The padding for DG operations is studied in Section 4.1.

The kernels of this implementation, corresponding to steps 2, 4 and 6, perform only data transfers and algebraic operations that are local to nodes or face nodes. The volume and update kernels are implemented following the one-node-per-thread strategy, with  $K_{\text{blkV}}$  and  $K_{\text{blkU}}$  elements per thread block. In contrast with the previous implementations, the surface kernel iterates over all the interfaces of the mesh. Each thread computes the numerical fluxes corresponding to one face node for both sides of the interface, and each thread block deals with  $K_{\text{blkS}}$  interfaces.

#### 4. Performance results

The different implementations are tested and profiled in a basic setting: the time stepping of an initial solution on a given mesh. We consider polynomial degrees ranging from 1 to 8 with, for each degree, a mesh corresponding to approx. 2 millions nodes. All the results therefore correspond to the same number of discrete unknowns (approx. 8 and 18 millions for the acoustic and elastic models, respectively). The computations are performed in single precision.

In Section 4.1, we discuss the memory storage of the SGEMM routine for the DG operations required by the third implementation. We then profile the SGEMM routine, report the arithmetic throughput and the memory bandwidth, and combine them in the roofline model (Section 4.2). In Section 4.3, we profile the DG kernels of the three implementations for the acoustic case, and we compare the global performances of the implementations for both acoustic and elastic cases.

##### 4.1. Storage strategy for SGEMM routine

The performance of the SGEMM routine strongly depends on both the dimensions of matrices and their storage in memory. For the operations required by the DG implementation, better performances are obtained with a row-major storage for **A**, while a column-major storage is used for **B** and **C**. We have tested several padding strategies. Only a padding of both the leading storage dimension  $ldc$  and the matrix dimension  $m$ , with  $ldc=m$ , can significantly improve performances. Increasing  $ldc$  involves a larger memory storage for matrix **C**, while increasing  $m$  also adds dummy floating-point operations. Though these tunings artificially increase the required computational resources, they lead to better runtimes for the SGEMM routine. The dimensions of matrices and storing arrays for the different SGEMM calls are summarized in Table 3.

The matrix **C** corresponds to different arrays in our DG implementation:  $Q^{tmp}$  for the gradient product,  $R^p$  for the divergence product, and  $R^p$  and  $R^v$  for the lift products. The value to pad is  $3N_p$  for the temporary array  $Q^{tmp}$ , and  $N_p$  for the right-hand side arrays  $R^p$  and  $R^v$ . For the sake of consistency, the padding used for the right-hand side arrays is also used for the arrays  $Q^p$  and  $Q^v$ , which have the same kind of memory storage. Since  $Q^p$  and  $Q^{tmp}$  correspond to the matrix **B** of operations gradient and divergence, respectively, the parameter  $ldb$  of these operations has to be padded (see Table 3). This additional padding does not change the performance, and is made only for compatibility.

The unpadded and optimized padded values for  $N_p$  and  $3N_p$  are listed in Table 4. Padding  $N_p$  improves the runtime only over polynomial degree  $N > 5$ , while padding  $3N_p$  improves runtime for all degrees. For nearly all the cases, the best padding corresponds to increasing  $N_p$  and  $3N_p$  until the next power of 2. The single exception is for  $3N_p$  at the seventh degree, where the next

**Table 3**

Dimensions of matrices for the four SGEMM operations  $C = \alpha AB + \beta C$ . According to BLAS terminology, the dimensions of **A**, **B** and **C** are, respectively,  $m \times k$ ,  $k \times n$  and  $m \times n$ , and  $\alpha$  and  $\beta$  are scalars. Storage is row-major for **A** and column-major for both **B** and **C**.  $lda$ ,  $ldb$  and  $ldc$  are the leading dimensions of storing arrays.  $N_p$ ,  $N_{fp}$ ,  $N_{faces}$  and  $K$  are, respectively, the number of nodes per element, the number of elements in the mesh, the number of faces per element and the number of elements in the mesh. For the lift operation,  $N_{fit}$  is the number of fields to lift (1 for  $p$  and 3 for  $v$ ).

Name	$m$	$n$	$k$	$lda$	$ldb$	$ldc$
Gradient	$(3N_p)_{pad}$	$K$	$N_p$	$N_p$	$(N_p)_{pad}$	$(3N_p)_{pad}$
Divergence	$(N_p)_{pad}$	$K$	$3N_p$	$3N_p$	$(3N_p)_{pad}$	$(N_p)_{pad}$
Lift	$(N_p)_{pad}$	$N_{fit}K$	$N_{faces}N_{fp}$	$N_{faces}N_{fp}$	$N_{faces}N_{fp}$	$(N_p)_{pad}$

**Table 4**

Unpadded and optimum padded values for  $N_p$  and  $3N_p$  when using the SGEMM routine for the DG operations. The padded values have been obtained by minimizing the runtimes for DG settings corresponding to approx. 8 millions discrete unknowns. Gray cells correspond to pads leading to increases of dimensions larger than 50%. No padding is used for  $N_p$  from the first to the fifth polynomial degree.

$N$	$N_p$	$(N_p)_{pad}$	$3N_p$	$(3N_p)_{pad}$
1	4	4	12	16
2	10	10	30	32
3	20	20	60	64
4	35	35	105	128
5	56	56	168	256
6	84	128	252	256
7	120	128	360	384
8	165	256	495	512

multiple of 32 is better. For small polynomial degrees ( $N \leq 5$ ), we have observed speedups between 1.1 and 1.5 for the gradient operation. The paddings do not affect the other operations. For higher degrees, speedups are between 2.1 and 3.2 for the gradient operation and between 1.4 and 1.8 for the others. In some cases (gray cells in Table 4), these paddings lead to an increase of the size of the system larger than 50%.

##### 4.2. Profiling of SGEMM routine for DG operations

To evaluate hardware utilization, we compare both arithmetic throughput and memory bandwidth of kernels to the theoretical peak values provided by the constructor, which are, respectively, 4616 GFLOP/s (single precision) and 224 GB/s for Nvidia's GTX980. The number of floating-point operations required for the general matrix multiplication is

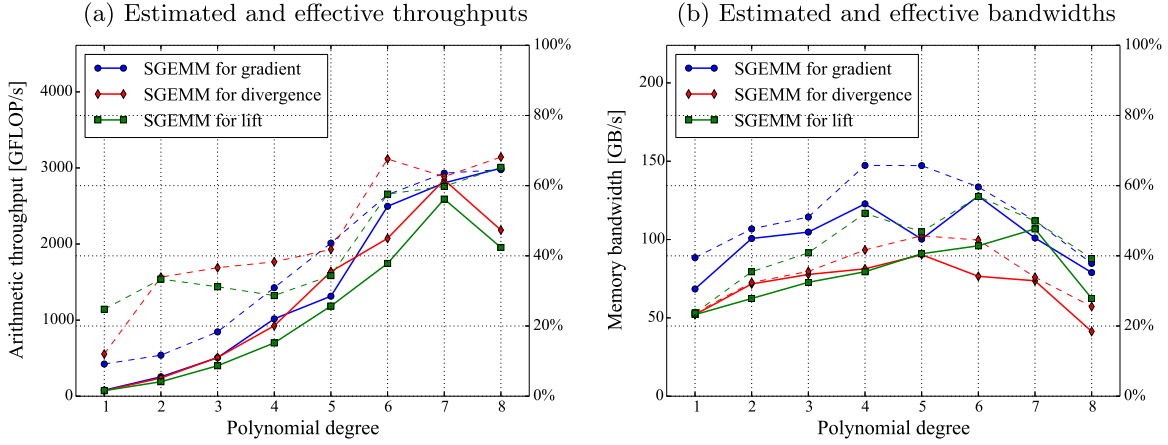
$$\#(\text{FLOP}) = 2mn(k + 1)$$

and the number of bytes transferred from and to the global memory is

$$\#(\text{Byte}) = 4(mk + nk + 2mn),$$

where the dimensions  $m$ ,  $n$  and  $k$  are not padded. Dividing these values by the runtime of the routine provides *estimated arithmetic throughput* and *estimated memory bandwidth*, respectively. These metrics give information about the performances for the requested operations, but they assume that there are no dummy floating-point operations and that data is always useful and transferred only once. However, optimization strategies, such as padding, can artificially increase the work really performed by the device. To evaluate that work, we also consider the *effective arithmetic throughput* and the *effective memory bandwidth*, which are obtained using metrics provided by Nvidia's profiler `nvprof`. The effective arithmetic throughput is computed using the number of floating-point operations given by `flop_count_sp`, and the effective memory bandwidth is obtained by summing `dram_read_throughput` and `dram_write_throughput`.

Fig. 1 shows the estimated and effective performances of cu-BLAS SGEMM routine for the DG operations presented in Section 3.3. Since the performance of the lift operation is similar for pressure and velocity fields, we show the results only for the pressure field. For all the operations, the estimated arithmetic throughput is far smaller than the effective value for low degrees, especially for divergence and lift operations, while  $m$  is not padded. Large differences are also observed at high degrees when the padding significantly increases  $m$ : for the gradient operation with  $N=5$  and for both divergence and lift operations with  $N=6$  and 8. In particular, the estimated throughput significantly decreases from  $N=7$  to  $N=8$  for both divergence and lift operations, while



**Fig. 1.** Arithmetic throughput (a) and memory bandwidth (b) for the SGEMM routine for DG operations with several polynomial degrees and, for each degree,  $N_p K \approx 2$  millions. Continuous lines correspond to estimated performances (i.e. considering only requested operations), while discontinuous lines are for effective performances (i.e. considering all the operations achieved by the device).

the effective throughput slightly increases. This difference of behavior is clearly related to the large number of dummy operations introduced by the large padding required for  $N=8$ , while the padded and unpadded dimensions are very close for  $N=7$ . Similar differences between estimated and effective memory bandwidths are also observed for cases with large padding.

In the remainder, we consider only estimated arithmetic throughput and memory bandwidth. Though these values underestimate the real work of the device, they allow us to compare different implementations without counting potential dummy operations and useless data transfers.

For all operations, the estimated arithmetic throughput is very small for low degrees (from few percents to 20% of the peak performance between  $N=1$  and 4) and grows until approximately 60% for  $N=7$ . The largest throughput, 65%, is obtained with the gradient operation for  $N=8$ . The estimated memory bandwidth increases for lower degrees and decreasing for higher degrees. The bandwidth reaches 54–57% of the peak performance (for  $N=4$  and  $N=6$ ) for the gradient operation, while the other operations exhibit slightly worse performances.

The general behavior of both throughput and bandwidth can be explained using the roofline model. Because of the physical limitations of the device, the performance of any operation is theoretically bounded either by the throughput or by the bandwidth, but rarely by both together. The roofline model provides a

tool to evaluate the dominant bound, and how far we are from that bound (Williams et al., 2009). The arithmetic throughput is plotted as a function of the operational intensity, which is defined as

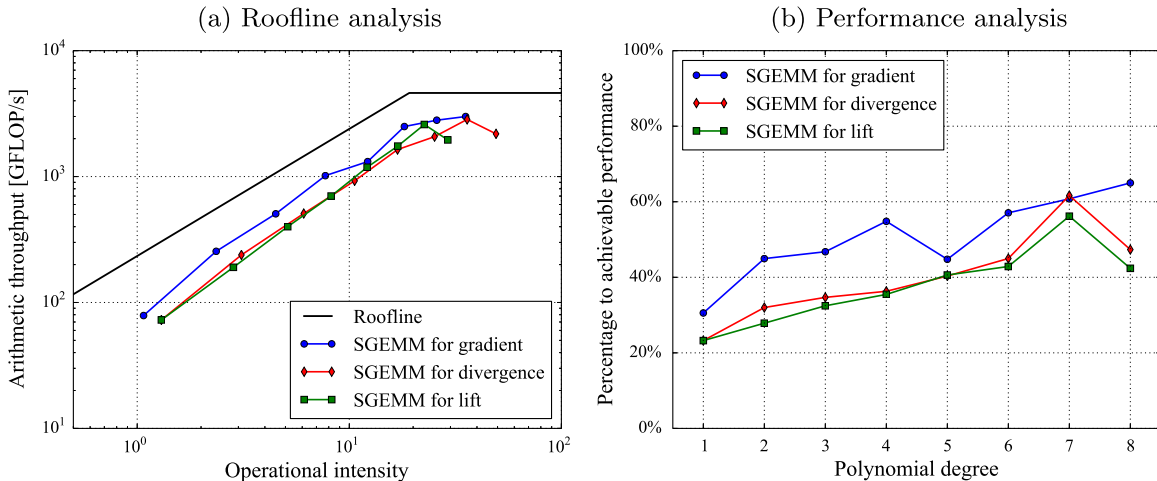
$$\text{operational intensity} = \frac{\#(\text{FLOP})}{\#(\text{Byte})} = \frac{2mn(k+1)}{4(mk+nk+2mn)}.$$

This metric determines the theoretical achievable throughput, which is

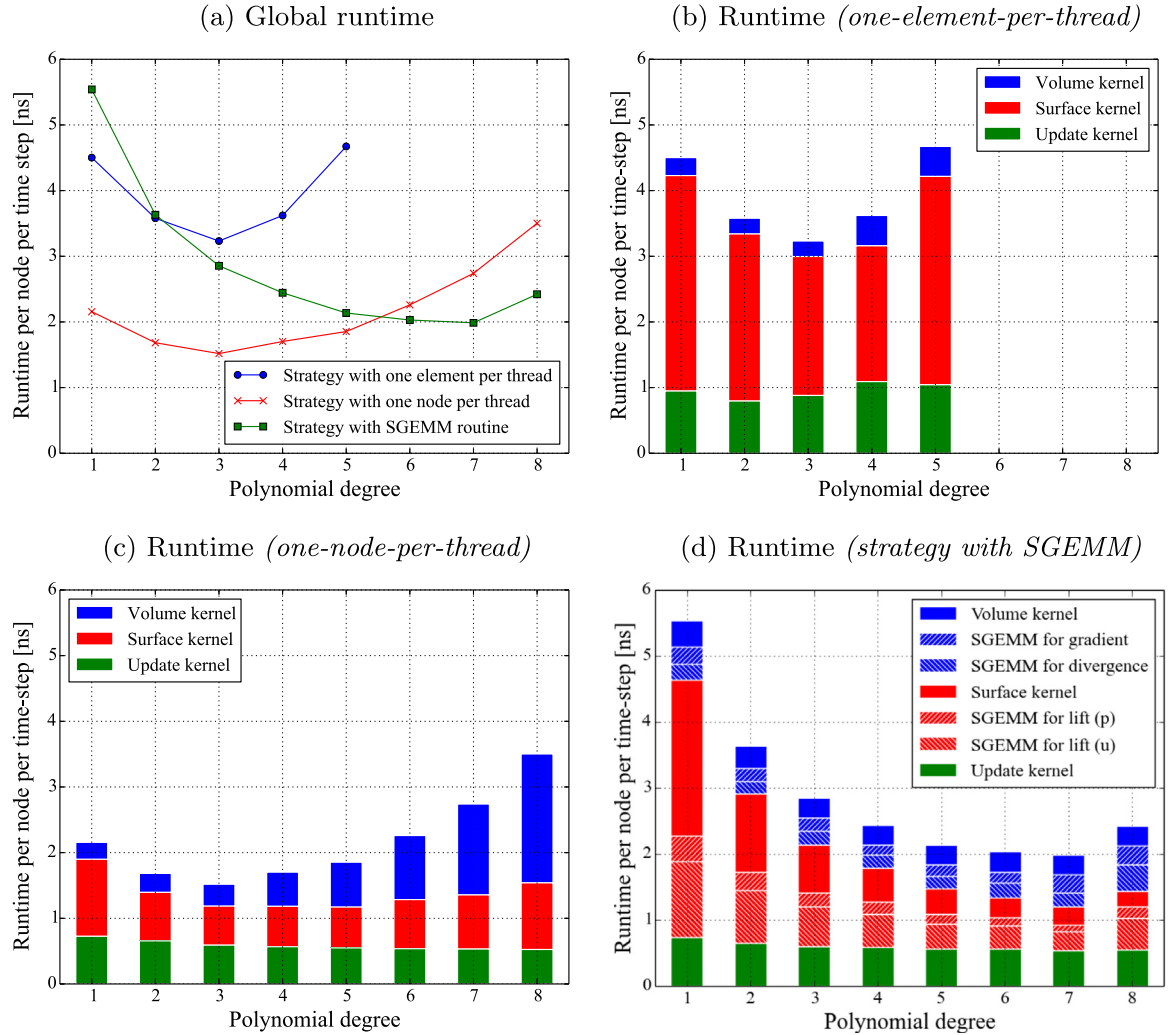
$$\begin{aligned} \text{achievable throughput} \\ = \min\{\text{peak bandwidth} \times \text{operational intensity}, \\ \text{peak throughput}\} \end{aligned}$$

The operation is bandwidth or throughput bounded if the operational intensity is small or large, respectively. Fig. 2a shows the curve of the achievable throughput (called the *roofline*) together with the obtained throughput for the different DG operations. The performance of the SGEMM routine for the DG operations are theoretically bounded by the bandwidth until the sixth or seventh degree, and by the arithmetic throughput beyond these polynomial degrees. This explains the low throughput observed for small degrees, as well as the stagnation of the throughput and the decaying memory bandwidth observed for the highest degrees.

Arithmetic throughput and memory bandwidth are representative of the implementation efficiency only when the



**Fig. 2.** Roofline analysis (a) of the SGEMM routine for DG operations, and percentage to achievable performance (b) considering the specific device. For every curves, each bullet corresponds to one polynomial degree. The leftmost bullet always corresponds to the first degree.



**Fig. 3.** Global runtimes per node per time step with the three DG implementations in the acoustic case (a), and runtimes kernel-by-kernel for each implementation (b)–(c)–(d). For each polynomial degree, a mesh corresponding to approx. 2 millions of nodes has been used. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

kernel is throughput or bandwidth bounded, respectively. To quantify the effectiveness of the SGEMM implementation in a unique way, we consider the percentage of the obtained throughput to its achievable value. When the kernel is bandwidth bound, this percentage actually also corresponds to the percentage of the obtained bandwidth to the peak bandwidth. This metric, that we call *percentage to achievable performance*, is shown in Fig. 2b. We observe that the performance of the implementation increases with the polynomial degree, but only for the cases without large padding already discussed above.

#### 4.3. Comparison and analysis of DG implementations

We compare and analyze the performance of the three DG implementations. The global runtime per node per time step is plotted in Fig. 3 for the acoustic case. We also show the detailed kernel-by-kernel for each implementation. For the one-element-per-thread strategy, results are shown only up to the fifth polynomial degree. Larger degrees were not feasible due to memory limitations. This is discussed later.

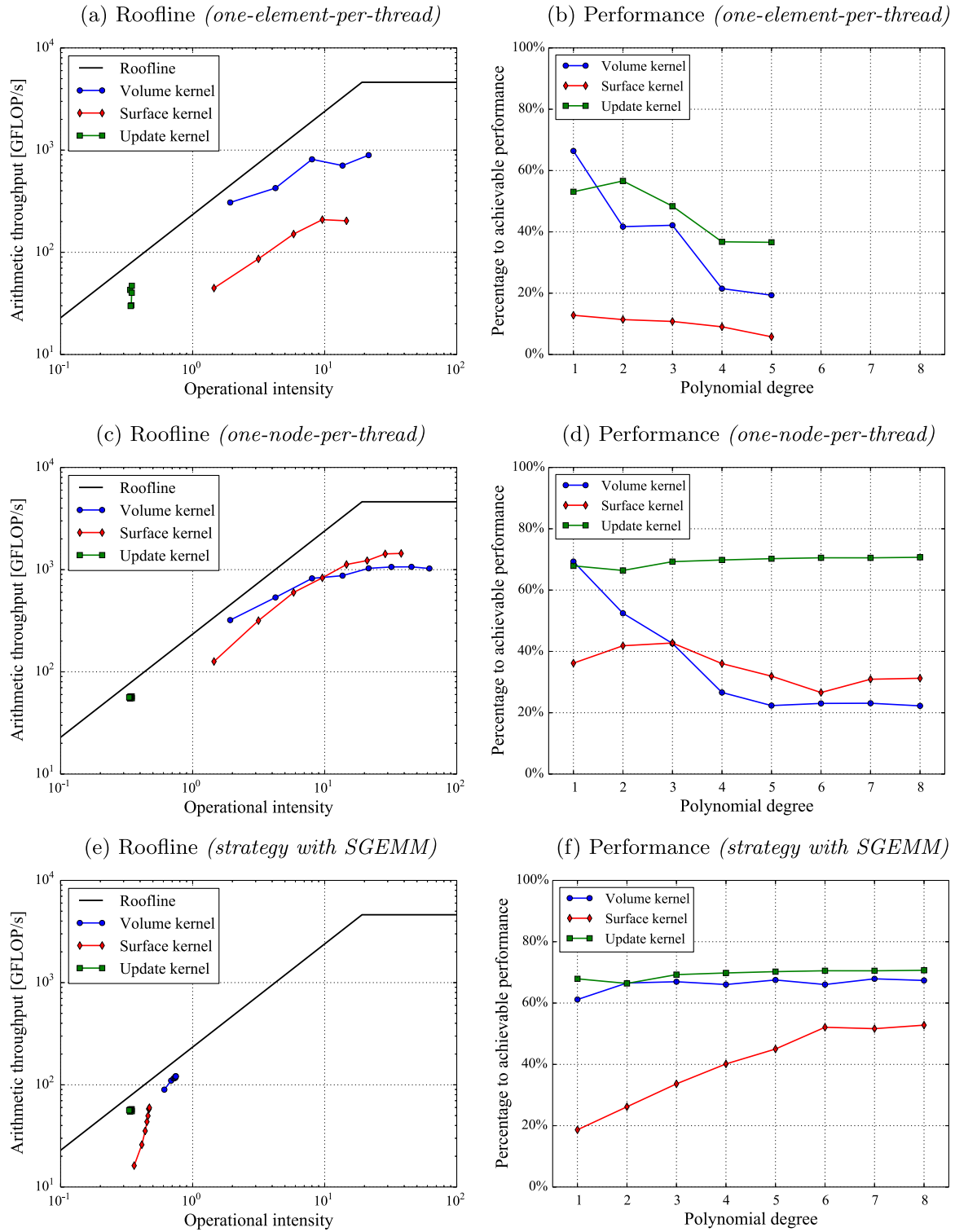
For all implementations, the global runtime per node decreases with polynomial degree until some minimum value is achieved. After this, the runtime increases with polynomial order. The minimum is reached at  $N=3$  for both one-element-per-thread and

one-node-per-thread strategies, and  $N=7$  for the strategy with the SGEMM routine. Until the fifth degree, the one-node-per-thread strategy provides the best performance. The runtime is larger by a factor two or more with the one-element-per-thread strategy. For higher degrees, the strategy with SGEMM is more efficient. Let us mention that these results are not necessarily correlated to the most suitable polynomial degree for applications. A complete performance analysis would include discussions of accuracy and time stepping. For instance, higher polynomial degrees allow for a better representation of high frequency modes, but they also reduce the allowed time step. Such an analysis is out of the scope of this paper.

In order to explain these results and to identify some bottlenecks in each implementation, we present the roofline and performance analyses of all the kernels in Fig. 4. Some statistics provided by Nvidia's compiler `nvcc` (allocated registers, local memory and shared memory) and Nvidia's profiler `nvprof` (occupancy with `achieved_occupancy` and hit rate for global loads with `global_hit_rate`) are listed in Table 5, together with the optimum numbers of elements per thread block  $K_{blk}$ . All the kernels have been tuned and the  $K_{blk}$ 's optimized to minimize the runtime as much as possible.

The roofline analyses show that all the kernels are bandwidth bound, except those that perform matrix–vector products with a





**Fig. 4.** Roofline and performance analyses of kernels for the different strategies in the acoustic case. For every curves, each bullet corresponds to one polynomial degree. The leftmost bullet always corresponds to the first degree.

large polynomial degree. All the update kernels and both volume and surface kernels of the strategy with SGEMM have small constant operational intensities. These kernels mainly perform streaming operations, and require less than one floating-point operation per transferred byte. The volume and surface kernels of both one-element-per-thread and one-node-per-thread strategies perform matrix-vector products, with which the number of required floating-point operations increases with the polynomial

degree. These kernels are in the bandwidth bound regime until  $N=4$  (volume kernel) or  $N=5$  (surface kernel), and in the throughput bound regime beyond.

We first analyze the performance of the one-element-per-thread kernels. The runtime of the volume kernel is very low in comparison to the runtime corresponding to the same operation with the other strategies (blue areas in Fig. 3). However, the update kernel does not perform as well as the other versions, and the

**Table 5**

Profiled statistics of each kernel for the different strategies in the acoustic case. The number of threads per thread block is always 256 for the one-element-per-thread strategy. There is no local memory allocated (lmem) with the one-node-per-thread strategy and the strategy with SGEMM.

Volume kernel (*one-element-per-thread*)

$N$	reg.	lmem	smem	occ.	gbl.h.
1	56	0	0.19	0.45	53%
2	64	0	1.17	0.35	51%
3	128	0	4.69	0.24	51%
4	186	0	14.35	0.12	51%
5	255	0.02	36.75	0.12	51%

Surface kernel (*one-element-per-thread*)

$N$	reg.	lmem	smem	occ.	gbl.h.
1	116	0	0.19	0.24	27%
2	149	0	0.94	0.12	24%
3	225	0	3.12	0.12	24%
4	255	0.07	8.20	0.12	24%
5	255	0.41	18.37	0.12	25%

Update kernel (*one-element-per-thread*)

$N$	reg.	lmem	smem	occ.	gbl.h.
1	72	0.07	0.05	0.36	52%
2	214	0.16	0.09	0.12	50%
3	255	0.38	0.16	0.12	50%
4	40	0.55	0.23	0.74	50%
5	40	0.88	0.33	0.71	49%

Volume kernel (*one-node-per-thread*)

$N$	$K_{\text{blk}}$	reg.	smem	occ.	gbl.h.
1	16	32	1.69	0.93	76%
2	16	35	3.19	0.88	91%
3	11	37	3.91	0.61	95%
4	5	32	2.95	0.90	97%
5	9	37	8.26	0.73	95%
6	3	37	4.07	0.74	94%
7	4	37	7.67	0.67	91%
8	3	32	7.86	0.98	87%

Surface kernel (*one-node-per-thread*)

$N$	$K_{\text{blk}}$	reg.	smem	occ.	gbl.h.
1	11	32	2.15	0.67	62%
2	2	32	0.58	0.95	75%
3	2	32	0.83	0.92	80%
4	2	31	1.14	0.93	84%
5	1	31	0.76	0.94	76%
6	9	32	8.79	0.89	85%
7	7	32	8.59	0.88	83%
8	5	31	7.54	0.85	82%

Volume kernel (*strategy with SGEMM*)

$N$	$K_{\text{blk}}$	reg.	smem	occ.	gbl.h.
1	8	27	0.34	0.49	41%
2	2	27	0.09	0.48	48%
3	1	27	0.04	0.48	40%
4	1	27	0.04	0.91	44%
5	1	27	0.04	0.91	50%
6	1	27	0.04	0.90	46%
7	1	27	0.04	0.92	50%
8	1	27	0.04	0.85	50%

Surface kernel (*strategy with SGEMM*)

$N$	$K_{\text{blk}}$	reg.	smem	occ.	gbl.h.
1	8	26	0.47	0.50	59%
2	4	26	0.33	0.50	53%
3	2	26	0.23	0.49	55%
4	1	26	0.15	0.49	52%
5	1	26	0.20	0.49	63%
6	1	26	0.25	0.49	59%
7	1	26	0.32	0.94	58%
8	1	26	0.39	0.93	62%

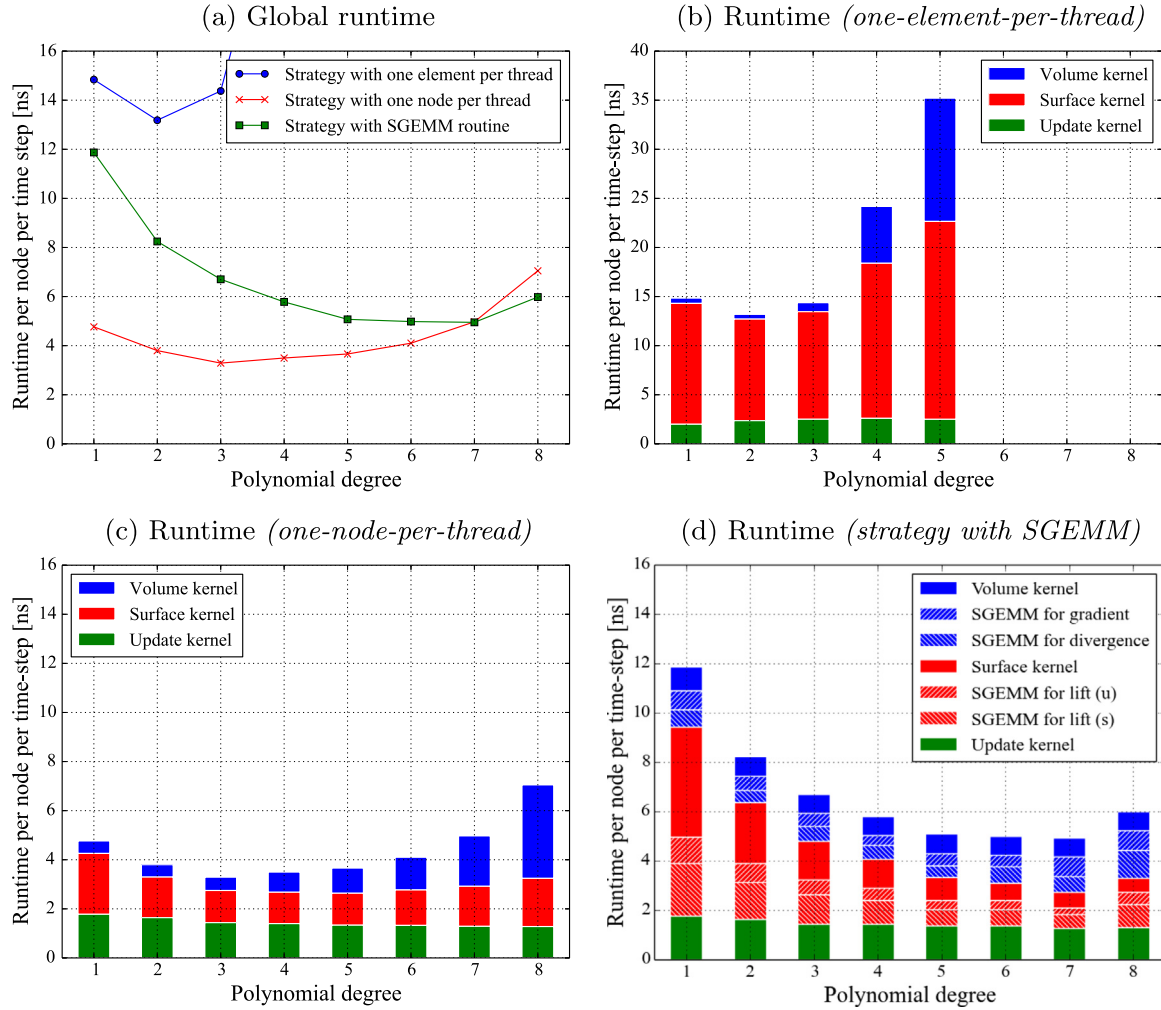
Update kernel (*one-node-per-thread and strategy with SGEMM*)

$N$	$K_{\text{blk}}$	reg.	smem	occ.	gbl.h.
1	16	30	1.00	0.87	53%
2	16	32	2.5	0.88	48%
3	10	32	3.12	0.77	53%
4	2	32	1.09	0.93	51%
5	1	32	0.88	0.91	58%
6	1	32	1.31	0.92	55%
7	1	32	1.88	0.88	56%
8	1	32	2.58	0.87	56%

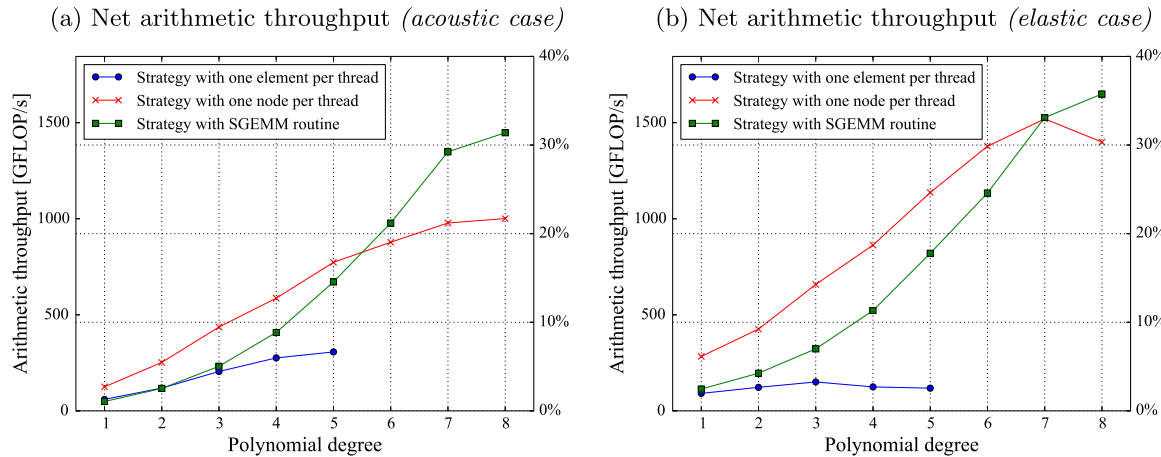
$N$	Polynomial degree
$K_{\text{blk}}$	Number of thread per thread block
reg.	Number of register per thread
lmem	Local memory allocated per thread [KB]
smem	Shared memory allocated per thread block [KB]
occ.	Occupancy
gbl.h.	Hit rate for global loads

surface kernel gives very bad results. A major bottleneck of those kernels is the storage required in local and shared memory. This storage increases with the polynomial degree  $N$ . The maximum number of registers per thread for the device is not sufficient to

store the local data from  $N=5$  for the volume kernel, from  $N=4$  for the surface kernel and for all polynomial degrees for the update kernel. This causes register spilling where local data is stored global memory (eventually cached in L1 or L2), which increases



**Fig. 5.** Global runtimes per node per time step with the three DG implementations in the elastic case (a), and runtimes per node kernel-by-kernel for each implementation (b)–(c)–(d). For each polynomial degree, a mesh corresponding to approx. 2 millions of nodes has been used.



**Fig. 6.** Net arithmetic throughput of the acoustic (a)–(b) and elastic (c)–(d) implementations. The net arithmetic throughput is obtained by dividing the total number of FLOP required per time step by the runtime required for one time step update.

latency. For  $N \geq 6$ , the shared memory required by the volume kernel is larger than the maximum allowed (48 KB), and the strategy cannot be used. The poor performance of the surface kernel is also partly explained by non-coalescing memory transfers. With this kernel, each thread has to load data corresponding to one element and its neighbors. Because the memory accesses are not aligned with the thread indexing for the neighbor

elements, the memory transfers cannot coalesce. The hit rate for global loads, 24–27% (see Table 5), is far smaller than for the other kernels. We have observed that this rate rises until approx. 50% if the memory transfers corresponding to the neighbor elements are removed.

With the one-node-per-thread strategy, the surface kernel is the most expensive kernel for small polynomial degrees, while the

volume kernel takes most of the runtime for large degrees (see Fig. 3c). For small degrees, the performance of the surface kernel is less efficient than for the volume kernel (see Fig. 4d), and it requires more floating-point operations (not shown for the sake of brevity). As  $N$  increases, the percentage of achievable performance of both kernels decreases, and reaches a plateau around 23% (volume kernel) and 30% (surface kernel) in the throughput bounded region. Over  $N=5$ , the volume kernel requires more floating-point operations than the surface kernel, which explains the larger runtime. The one-node-per-thread update kernel, which is also used for the strategy with SGEMM, exhibits a constant and high percentage of achievable performance (around 70%). The volume kernel of that strategy also has a similar performance (around 67%). For the surface kernel, the performance is bad for small degrees, but it increases until a plateau around 52% for  $N \geq 6$ .

The performance results then are consistent with the observed runtimes: both volume and surface kernels perform better for small degrees with the one-node-per-thread strategy, while both surface kernel and SGEMM routine perform better for large degree for the strategy with SGEMM. The profiled statistics of the kernels are quite good. There is no register spilling, and both the number of registers per thread and the shared memory per thread block are reasonable. Increasing the number of elements per thread block helps to improve the occupancy for small polynomial degrees. The occupancy and the hit rate for global loads cannot explain the variations of performance that are observed. We have obtained from NVIDIA's profiler `nvprof` that most of the stalls occur because of data requests (metric `stall_data_request`) and execution dependencies (metric `stall_exec_dependency`), which are difficult to avoid.

The observations made for the acoustic case also apply to the elastic case, which requires more floating-point operations and memory transfers. We show the global runtime per node for the three elastic implementations and the detailed kernel-by-kernel runtimes in Fig. 5. The simulations have been done on the same meshes. The one-node-per-thread strategy remains the most efficient for small degrees. The strategy with SGEMM is as efficient as the one-node-per-thread strategy at  $N=7$ , and is better for  $N=8$ . The one-element-per-thread strategy is again very bad, with results far worse than before. Since the operations require a larger local memory, register spilling occurs for  $N$  smaller than with the acoustic case, which worsens the results.

The one-node-per-thread strategy is only 1.8–2.25 times slower than for the acoustic case, while the number of fields increases by a factor 2.25. This is partly explained by the operational intensity that is larger in the elastic case for both volume and surface kernels. The strategy with SGEMM is 2.14–2.49 times slower than in the acoustic case.

Finally, to have an idea of the global performance of each strategy as a whole, we plot the net arithmetic throughput of each implementation for both acoustic and elastic cases in Fig. 6. The net arithmetic throughput is obtained by dividing the total number of floating-point operations required for one full time step by the corresponding runtime required. The implementation with SGEMM reaches 31.4% of the peak throughput for the acoustic case, and 35.7% for the elastic case. A larger increase is observed with the one-node-per-thread strategy, from 21.7% to 33%. This made of this strategy an interesting candidate for DG schemes requiring denser computations.

## 5. Conclusion

We have presented and analyzed three GPU implementations for time-domain discontinuous Galerkin simulations of acoustic and elastic waves. Two of them are based on tailored kernels

programmed by associating each thread to one element or one node, following strategies described by Klöckner et al. (2009) and Fuhry et al. (2014), respectively. We have also considered an alternative implementation with a specific partition of work which makes use of the SGEMM routine of an external BLAS library. All the implementations have been optimized and compared in the same computational framework with a three-dimensional benchmark.

The computational results highlight the strong performance of the one-node-per-thread kernels until  $N=5$  for acoustic and  $N=7$  for elastic waves. The strategy with SGEMM performs better for higher polynomial degrees, though it requires more data transfers and more data storage in global memory. The one-element-per-thread implementation does not work well for three-dimensional problems in our framework. We have analyzed both the SGEMM routine and the acoustic DG kernels using the roofline model, and we have identified bottlenecks for each computational strategy.

In the perspective of large-scale applications, it is essential to combine the selected implementation with a multi-rate time stepping scheme and parallel computation with several GPUs. The one-node-per-thread implementation has already been adapted to multi-rate time stepping (Gandham et al., 2015; Gödel et al., 2010) and multi-GPU computation (Modave et al., 2015a). The implementation with SGEMM can be adapted in very similar ways. In the future, we plan to investigate kernels for anisotropic wave propagation and artificial boundary conditions.

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